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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,854	08/26/2003	Fredrick W. Trafton	TI-35749	2827

23494 7590 07/29/2004

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EXAMINER

LAXTON, GARY L

ART UNIT PAPER NUMBER

2838

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/646,854

Applicant(s)

TRAFTON ET AL.

Examiner

Gary L. Laxton

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/27/03</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claims 1-12 are objected to because of the following informalities:

Claim 1 recites the limitation "the feedback circuitry" in line 13. There is insufficient antecedent basis for this limitation in the claim. Claims 2-12 inherit the same.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "an output terminal" in line 6. There is insufficient antecedent basis for this limitation in the claim. It is unclear if the applicant is referring to the "at least one output terminal" recited in line 2 or whether it is another output terminal.

Claim 1 recites the limitation "an input terminal" in line 7. There is insufficient antecedent basis for this limitation in the claim. It is unclear if the applicant is referring to the "at least one input terminal" recited in line 3 or whether it is another input terminal. Claims 2-12 inherit the same from claim 1.

Claim 2 recites "the input terminal" in line 3. It is unclear which input terminal the applicant is referring since it is unclear whether there is more than one terminal.

Claims 2-12 inherit the same from claim 1.

Claim 13 is drafted in the alternative. It is also considered vague and indefinite since the applicant has recited limitations for both modes yet has not positively recited that the power supply switches between modes nor indicated any triggering event that would suggest that the power supply does indeed switch between two different modes. As the claim stands presently, it is unclear if the power supply does switch modes and when does it switch; or, if the power

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supply is merely configurable in one mode but is capable of being configured in the other mode but not both. Claims 14-19 inherit the same through dependency.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanouda et al (US 6,489,756).

The rejections are made based on the best understanding of the claim language due to the 112 2nd paragraph issues noted above.

Claims 1 and 11; Kanouda et al discloses a circuit, comprising: a plurality of terminals including at least one output terminal (Vout) and at least one input terminal (Vin); and a configurable voltage regulator (figure 1) operable in a first mode (linear) or a second mode (switching), comprising: output driver circuitry (14), control circuitry (7, 9, 10, 11, 12, 52), having an output coupled to the output driver circuitry, and including a plurality of elements; configuration circuitry (12, 13, 52), for receiving a configuration signal; and at least one configuration switch (12), for selectably coupling elements of feedback circuitry to the output driver circuitry responsive to control signals from the configuration circuitry.

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However, Kanouda et al do not disclose the circuit being integrated. It has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the circuit of Kanouda et al integrated in order to simplify circuit design, reduce manufacturing costs and reduce the overall size of the power supply.

Claim 13; Kanouda et al disclose a method of generating a regulated voltage, comprising the steps of: configuring a configurable voltage regulator either in a linear regulator mode or a switching regulator mode, the configurable voltage regulator comprising output drive circuitry having an output at a drive terminal, and comprising an error amplifier having an input coupled to a sense terminal; connecting the gate of a transistor to the drive terminal; in the switching regulator mode: connecting an external network including an inductor to the transistor, the external network producing the regulated voltage; connecting the error amplifier of the voltage regulator to the external network, so that the error amplifier receives a voltage corresponding to the regulated voltage.

However, Kanouda et al do not disclose the circuit being integrated. It has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove works*, 150 U.S. 164 (1893).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the circuit of Kanouda et al integrated in order to simplify circuit design, reduce manufacturing costs and reduce the overall size of the power supply.

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8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanouda et al (US 6,489,756) in view of Esteves et al (US 6,724,174).

Claim 2; Kanouda et al discloses the claimed subject matter in regards to claim 1 supra, except for the configuration circuitry comprises: a configuration amplifier, having a first input connected to the input terminal, and having a second input connected to a reference voltage, the configuration amplifier having an output coupled to the at least one configuration switch.

Esteves et al teaches configuration circuitry comprising a configuration amplifier (261), having a first input connected to an input terminal, and having a second input connected to a reference voltage (V_{th}), the configuration amplifier having an output coupled to the at least one configuration switch (266).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Kanouda et al to include configuration circuitry that comprises a configuration amplifier, having a first input connected to the input terminal, and having a second input connected to a reference voltage, the configuration amplifier having an output coupled to the at least one configuration switch to change modes of operation as taught by Esteves et al.

Claim 3; Kanouda et al discloses the claimed subject matter in regards to claim 1 supra, except for wherein the at least one configuration switch is in the first position responsive to a voltage at the input terminal being above the reference voltage and is in the second position responsive to a voltage at the input terminal being below the reference voltage.

Esteves et al teaches Esteves et al teaches configuration circuitry comprising a configuration amplifier (261), having a first input connected to an input terminal, and having a

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second input connected to a reference voltage (V_{th}), comprising a configuration amplifier (261), having a first input connected to an input terminal, and having a second input connected to a reference voltage (V_{th}), and wherein the configuration circuitry is responsive to a voltage at the input terminal being above the reference voltage and is responsive to a voltage at the input terminal being below the reference voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Kanouda et al to include configuration circuitry with the at least one configuration switch in the first position and being responsive to a voltage at the input terminal being above a reference voltage and is in a second position and responsive to a voltage at the input terminal being below the reference voltage as suggested by Esteves et al in order to change modes based on a threshold voltage as taught by Esteves et al.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanouda et al (US 6,489,756) in view of Basso et al (US 6,452,368).

Kanouda et al discloses the claimed subject matter in regards to claim 1 supra, except for wherein the configuration circuitry comprises a writable configuration register, coupled to the at least one configuration switch, for receiving and storing configuration data indicating the selected mode.

Basso et al teaches using a microcontroller to control the mode selection. Microcontrollers inherently comprise memory (ROM and RAM) (i.e. writable register) and receive and store data.

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Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize configuration circuitry that comprises a writable configuration register, coupled to the at least one configuration switch, for receiving and storing configuration data indicating the selected mode in order to program the operating characteristics of the power supply and to utilize computer control to increase power conversion efficiency as taught by Basso et al.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanouda et al (US) in view of Matsuyama (US 5,969,512).

Kanouda et al discloses the claimed subject matter in regards to claim 1 supra, except for a second voltage regulator, having an output coupled to a second output terminal, for generating a negative polarity regulated voltage.

Matsuyama teaches coupling two regulators together and wherein the second regulator, has an output coupled to a second output terminal, for generating a negative polarity regulated voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to couple two regulators together wherein the second regulator, has an output coupled to a second output terminal, for generating a negative polarity regulated voltage as suggested by Matsuyama in order to provide multiple voltages to a load that demands more than one voltage.

Allowable Subject Matter

11. Claims 5-10 and 14-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claims 5-10; prior art fails to disclose or suggest, inter alia, an integrated circuit having control circuitry that comprises: a first configuration switch for connecting the output of the error amplifier to the switching regulator control circuitry in a first position; a second configuration switch, for connecting the output of the switching regulator control circuitry in a first position; wherein the first and second configuration switches connect the output of the error amplifier to the output driver circuitry when in a second position; and wherein the first and second configuration switches switch to the first and second positions responsive to a signal from the configuration circuitry.

Claims 14-19; prior art fails to disclose or suggest, inter alia, a method of generating a regulated voltage comprising a configuring step that comprises: comparing a voltage at a first sense terminal to a fixed voltage; responsive to the comparing step determining that the voltage at the first sense terminal is in a first relationship related to the fixed voltage, controlling configuration switches to couple the output of the error amplifier to the output drive circuitry to configure the voltage regulator in the linear regulator mode; and responsive to the comparing step determining that the voltage at the first sense terminal is in a second relationship relative to

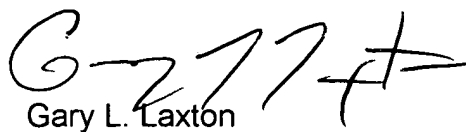
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the fixed voltage, controlling the configuration switches to couple the output of the error amplifier to the switching regulator control circuitry and to couple the switching regulator control circuitry to the output drive circuitry to configure the voltage regulator in the switching regulator mode.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Gary L. Laxton
Patent Examiner
Art Unit 2838

GLL